

CLAIMS

What is claimed is:

1. An integrated circuit semiconductor-on-insulator structure, comprising:
 - a pair of matched transistors, in a circuit stage which requires matched behavior of said pair; and
 - 5 a physical connection of semiconductor material which provides thermal conduction between respective bodies of said pair of transistors, but does not carry current during normal operation of said circuit stage; and
 - 10 an insulating material which totally surrounds at least part of said circuit stage.
2. The integrated circuit of Claim 1, wherein said circuit stage is an analog circuit stage.
3. The integrated circuit of Claim 1, wherein said circuit stage is a matched pair of current-sourcing P-channel transistors in a current mirror.
4. The integrated circuit of Claim 1, wherein said circuit stage is a cascode pair.

5. The integrated circuit of Claim 1, wherein said circuit stage is an input pair of a differential analog stage.
6. An integrated semiconductor-on-insulator circuit structure, comprising:
- a pair of transistors in an analog circuit stage which requires matched behavior of said pair;
 - 5 a physical connection of metallic material which provides thermal conduction between respective bodies of said pair of transistors, but does not carry current during normal operation of said circuit stage; and
 - an insulating layer beneath said pair;
 - 10 an insulating barrier substantially surrounding said pair and extending to said insulating layer .
7. The integrated circuit of Claim 6, wherein said analog circuit stage is a current mirror.
8. The integrated circuit of Claim 6, wherein said analog circuit stage is a matched pair of current-sourcing P-channel transistors in a current mirror.
9. The integrated circuit of Claim 6, wherein said physical connection comprises metal interconnects between said transistors of said pair.

10. An integrated semiconductor-on-insulator circuit structure,
comprising:
a plurality of matched transistors in an analog circuit stage which
requires matched behavior of said transistors;
- 5 wherein respective bodies of said transistors are formed from
different semiconductor sections, said sections being formed
on an insulating layer and at least partially separated by
insulating material;
- wherein said bodies are not tied to any fixed potential; and
- 10 wherein said bodies are thermally coupled by a connection of non-
insulating material.
11. The integrated circuit of Claim 10, wherein said bodies are electri-
cally coupled by a connection of non-insulating material.
12. The integrated circuit of Claim 10, wherein said analog circuit
stage is a current mirror.
13. The integrated circuit of Claim 10, wherein said connection of non-
insulating material is made from semiconductor material.
14. The integrated circuit of Claim 10, wherein said analog circuit
stage is a current mirror.
15. The integrated circuit of Claim 10, wherein said analog circuit
stage is a matched pair of current-sourcing P-channel transistors
in a current mirror.

16. A method of circuit operation, comprising the steps of:
providing a pair of matched transistors, in a circuit stage which
requires matched behavior of said pair; and
providing a physical connection of material which provides thermal
5 conduction between respective bodies of said pair of transis-
tors; and
surrounding said circuit stage with an insulating material.

17. The method of Claim 16, wherein said physical connection is of a
semiconductor material.

18. The method of Claim 16, wherein said circuit stage is an analog
circuit stage.

19. The method of Claim 16, wherein said physical connection does
not carry current during normal operation of said circuit stage.